WE CLAIM:

1. A semiconductor integrated circuit device comprising:

a clock-generating circuit that includes a variable delay circuit for producing second clock signals by delaying, by a predetermined delay time, first clock signals that are formed based upon clock signals input through an external terminal, and a control circuit for comparing the phase of third clock signals formed based on the second clock signals with the phase of the first clock signals and for so controlling the delay time that the difference between the phases is decreased; and

an internal circuit that operates in response to the second clock signals;

which are formed on a common semiconductor substrate;

wherein an element-forming region constituting the variable delay circuit is isolated from an element-forming region constituting the internal circuit; and

wherein the semiconductor integrated circuit device further includes:

a clock input circuit which receives the input clock signals and produces the first clock signals;

an output circuit that operates upon receiving the second clock signals;

a replica delay circuit for forming the third clock signals by delaying the second clock signals by the time corresponding to the delay times of the clock input circuit and of the output circuit; and

wherein the internal circuit includes the output circuit.

2. A semiconductor integrated circuit device comprising:

a clock-generating circuit that includes a variable delay circuit for producing second clock signals by delaying, by a predetermined delay time, first clock signals that are formed based upon clock signals input through an external terminal, and a control circuit for comparing the phase of third clock signals formed based on the second clock signals with the phase of the first clock signals and for so controlling the delay time that the difference between the phases is decreased; and

an internal circuit that operates in response to the second clock signals;

which are formed on a common semiconductor substrate;

wherein an element—forming region constituting the variable delay circuit is isolated from an element-forming region constituting the internal circuit;

wherein:

the delay time is controlled by an analog voltage;

the control circuit includes a first frequency-dividing circuit for forming fifth clock signals by dividing the frequency of the first clock signals, a second frequency-dividing circuit for forming sixth clock signals by dividing the frequency of the third clock signals, and a phase comparator circuit for producing control signals by comparing the phase of the fifth clock signals with the phase of the sixth clock signals, and a charge pump circuit that generates the analog voltage based upon the control signals;

wherein the fifth and sixth clock signals assume predetermined initial values when the clock-generating circuit is in operation; and

wherein the first and second frequency-dividing circuits and the phase comparator circuit are formed in an

element-forming region electrically isolated from an element-forming region where the variable delay circuit is formed.